



War-Winning Capabilities ... On Time, On Cost



F-16 Engine Testing in the Failed State A Summary of Lessons Learned April 2009

U.S. AIR FORCE

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Integrity - Service - Excellence







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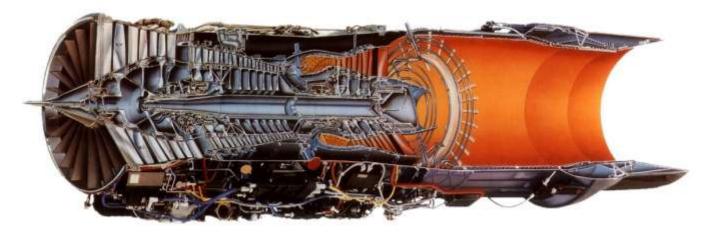


1. Overview of Test Objectives



Overview of Test Objectives





- Operation controlled by Engine Digital Control (EDC) hardware and software
- EDC software upgrade designed to reduce:
 - Stalls in high altitude/low Mach regime
 - False stall detections





- Demonstrate:
 - -High altitude/low Mach performance
 - -No adverse engine responses or operability produced by software update, including engine shutdown and airstarts
 - ie, testing in the 'FAILED STATE'





2. Background



F-16 Engine Testing in the Failed State







F-16 Engine Testing in the Failed State







F-16 Engine Testing in the Failed State



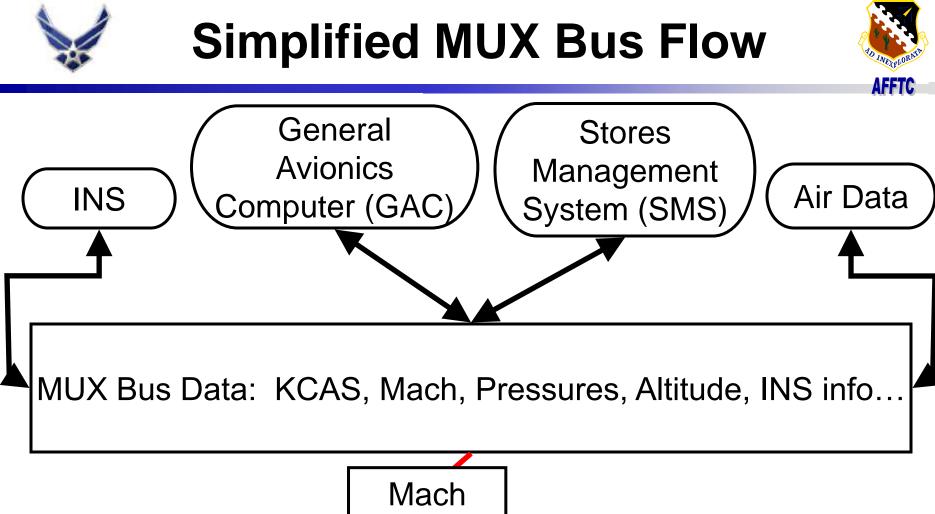
Provides electrics & hydraulics

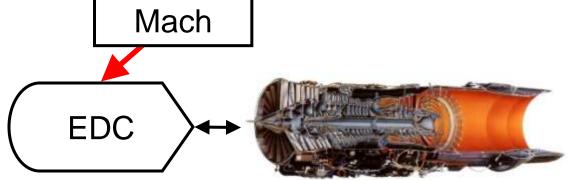
Hydrazine-Powered Emergency Power Unit (EPU)



- Partial hydraulic power
- Emergency electric power
 - -<u>Only Emergency</u> <u>Electrical bus is</u> <u>powered</u>



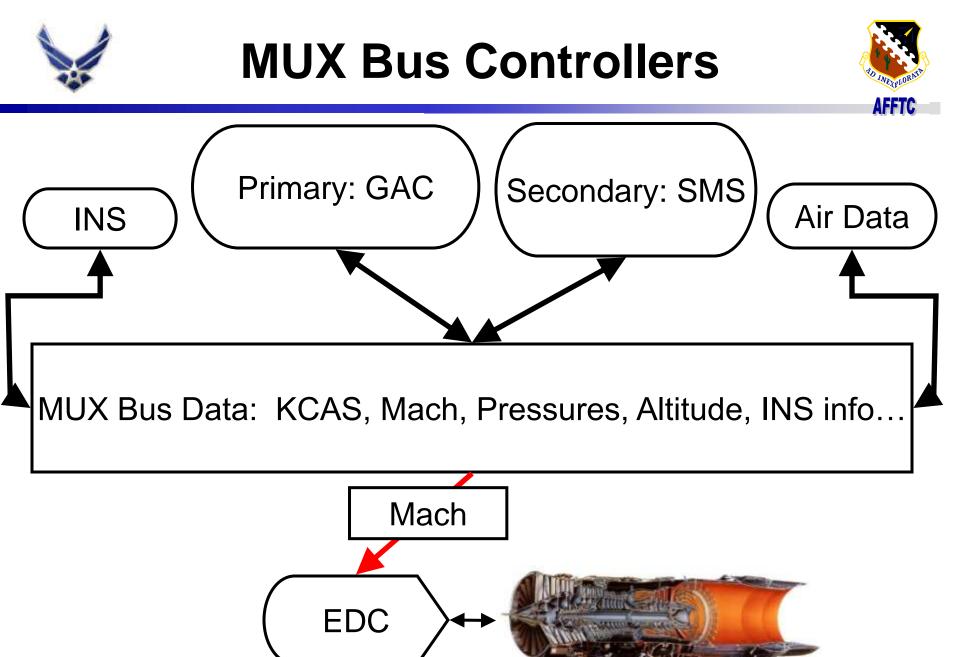
















SMS 'designed' to take over MUX bus control when:

- 1. GAC fails
- 2. EPU powering Emergency Electric bus
 - When the engine isn't operating!
 - GAC falls offline (load shedding)





Engine Operating Modes

- Primary (PRI)
 Mode
 - Max thrust and stall protection
 - Robust airstart envelope
 - AB available
 - Full nozzle control



Engine Operating Modes



- Primary (PRI) Mode
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 - Robust airstart envelope
 - AB available
 - Full nozzle control

- Secondary (SEC) Mode
 - EDC Failure
 - Possible engine failure during SEC reversion
 - Reduced stall protection and thrust (No AB)
 - Reduced airstart envelope
 - Nozzle stuck closed





3. First "Flight" Sequence of Events





- EDC software tested in integration lab
 - Including failed state testing with SMS as 2^Y MUX bus controller
- Flight-test proven EDC hardware – F-15 'sibling' project
- Robust ground runs in test aircraft
 - -MAX/MIL/Idle transients, etc
 - -NO failed state testing





- Normal ground ops
- MIL thrust takeoff
- Heart of envelope throttle transients and Mach sweep
- Airstart test points
 - -Heart of envelope
 - -High/slow edge of envelope







- Normal Start
- GAC failure due to internal hardware fault
- INS data dumps
- Control room reports MUX bus flooded with 'noise'
 - Including critical safety of flight/test parameters
- 10 mins into trouble shooting
 Engine reverts to SEC





Flight cancelled- back to the old drawing board!





4. Ramifications





- Airstart testing=
 - -EPU-ON
 - -GAC offline
- GAC failure in chocks inadvertently provided ground test of avionics in the failed state...
- And revealed some major issues with aircraft, avionics, and engine!



Ramifications



- INS dump
 - Complicates flame out landing execution
- MUX bus 'noise'
 - Monitoring of critical parameters in control room impeded
- Engine reversion to SEC
 - Worst case= engine failure / unable to restart engine
 - Best case= long, 'hot' landing





5. 'Investigation' Results



- Several test modifications over last two decades
 - Engine testbed
 - Flight control system testbed
 - Avionics testbed
- Block 25 F-16 subsequently modified to Block 40
- Formerly, INS was secondary MUX bus controller (vice SMS)





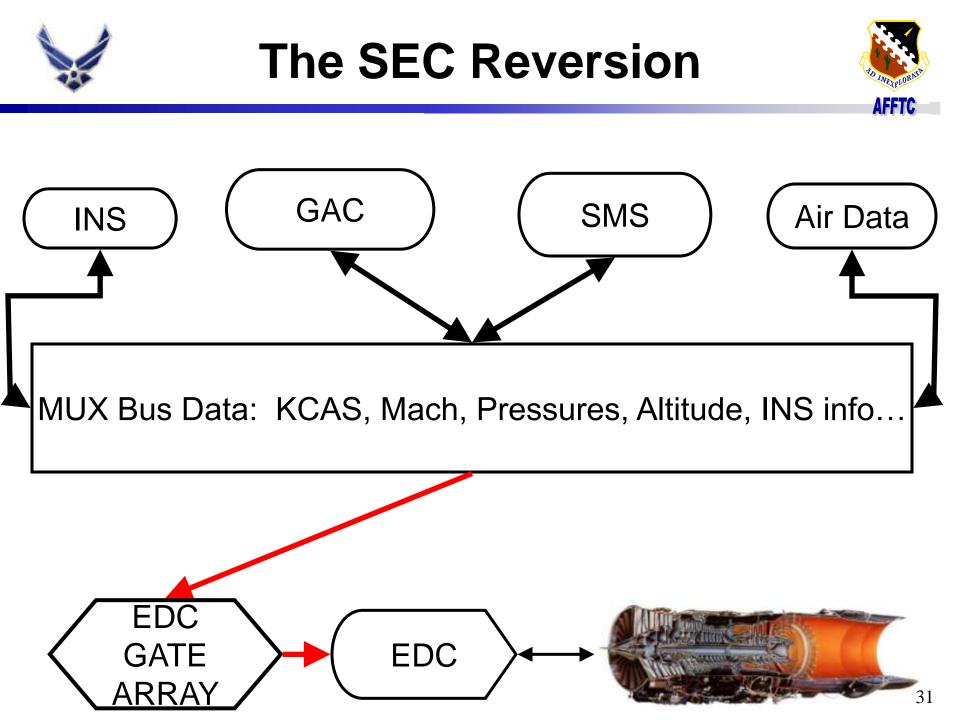
- Would NOT attempt 2^y MUX bus control
- Hard wired to aircraft battery during load shedding
- Reality:
 - INS 'fighting' with SMS for 2^y MUX bus control
 - 'Garbage' and 'Noise' on bus when GAC offline
 - Electrical failures resulting in INS dump when transferring to battery power

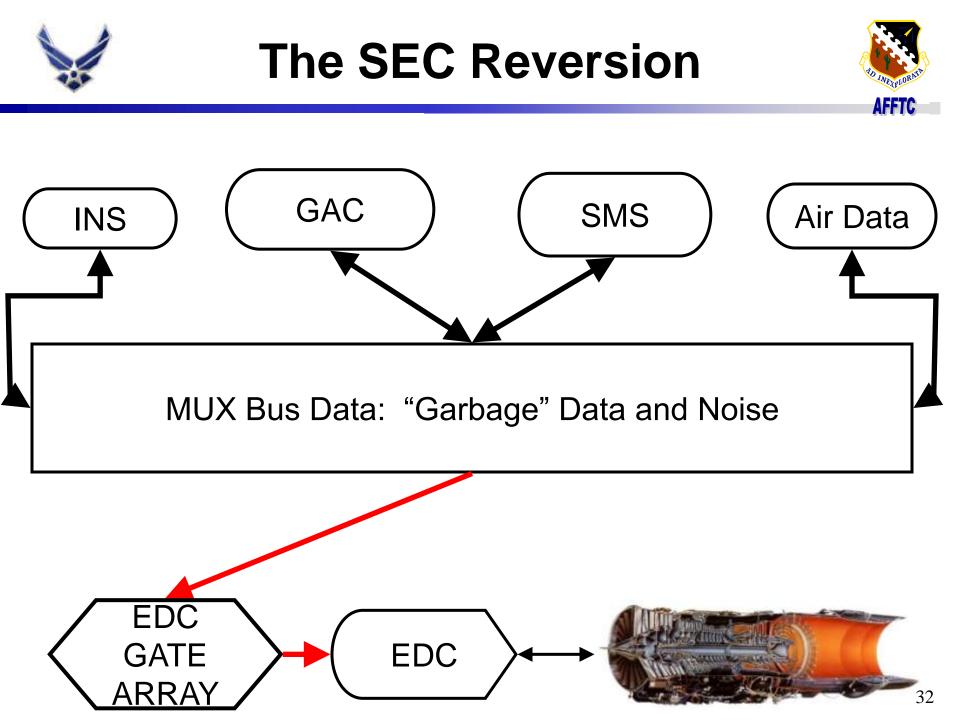






- Software under test using recently upgraded EDC hardware
 - -Flight tested
 - Operationally fielded
- Hardware upgrade
 - MUX bus data collected via 'Gate Array'
 - -Goal to enhance performance of future EDC









- Gate array recognized presence of 'garbage' data via BIT parity error logic
- Misinterpreted this as a EDC hardware failure vice MUX bus problem
- EDC shut down causing reversion to SEC 'as designed'





Aircraft Avionics Failures Driving Engine into Failure Mode!







6. Recommendations





1. If planning airborne tests in the failed state, conduct ground tests in the failed state

- Emulate avionics failed state conditions
- Activate EPU





2. Heavily modified test aircraft can generate surprises

- Lab tests used 'standard' block 40 F-16 avionics and architecture
- Actual test aircraft had been significantly modified in ways that affected testing in the failed state
- Operationally representative test aircraft?
- Critical review of all system modifications and ground testing essential





3. Never believe "that's impossible!"

- Initially, manufacturer categorically denied any link between GAC failure and SEC reversion
- Subsequent lab tests consistently reproduced the problem in presence of MUX 'noise'





4. The system under test may be the least of the worries

- EDC software worked as designed, flawlessly
- Safety issues caused by EDC hardware, which was not the system under test!





5. Take a cautious approach towards systems integration

- Good reason to have engine operation 'separated' from avionics
- Highly integrated designs:
 - Vectored thrust example
 - Flight control laws and computers
 - Air data systems
 - MUX buses
 - Engine operations and control laws





6. External safety oversight is critical

- Team eager to control MUX bus noise and 'get flying'
 - Reduce MUX bus loading via test GAC software
 - Treat symptom
- Oversight directed team to get the root cause before any more flights





7. Test points near the edge of the envelope hold other surprises

- Mach 2 run aborted at 1.8 due to airframe vibration
- Tail hook found slightly out of rig tolerance
- Appears as though aircraft hadn't been at this part of the envelope in two years





- INS problems corrected
- 'Clean' MUX bus data, even in failed state
 Therefore no SEC reversion concern

Epilogue

- Smooth flow of airstarts, throttle transients, and Mach sweep test points
- EDC software performed flawlessly, as designed
- Deficiency Report generated for design of EDC Gate Array / MUX bus interaction





Questions and Wrap Up